PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Akram et al.

Serial No.: 10/032,734

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For: MULTI-CHIP MODULE SYSTEM AND METHOD OF FABRICATION

Examiner: David E. Graybill

Group Art Unit: 2827

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AMENDMENT

Box NON-FEE AMENDMENT
Commissioner for Patents
Washington, D.C. 20231

Sir:

This amendment is in response to the Office Action of August 12, 2002, whose initial period of response is set to expire on November 12, 2002.

IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity.

Please amend the claims as follows:

1. A multi-chip module system comprising:

a substrate having at least a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat and having at least one other vacant position having, in turn, a predetermined configuration for locating a second semiconductor device thereat on the multi-chip module system; and

a first semiconductor device located in the at least first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; wherein said first semiconductor device has been burned in at said location on said substrate.

2. The multi-chip module system of claim 1, further comprising:

the at least one other vacant position having the predetermined configuration for locating the second semiconductor device thereat which is substantially the same as the predetermined configuration of the first position.

3. The multi-chip module system of claim 1, further comprising:

the at least one other vacant position having the predetermined configuration for locating the second semiconductor device thereat; and

the second semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

4. The multi-chip module system of claim 1, further comprising:

the at least one other vacant position having the predetermined configuration for locating the second semiconductor device thereat; and

the second semiconductor device having a second predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

5 A multi-chip module system comprising:

a substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat, and having at least one other vacant position having, in turn, a predetermined configuration for locating a third semiconductor device thereat on the multi-chip module system;

the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

the second semiconductor device located in the second position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic; wherein said first and second semiconductor devices have been burned in at said first and second positions, respectively, on said substrate.

6. The multi-chip module system of claim 4, further comprising:

the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat which is substantially the same as the predetermined configuration of the first position.

7. The multi-chip module system of claim 4, further comprising:

the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat; and

the third semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

8. The multi-chip module system of claim 4, further comprising:

the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat; and

the third semiconductor device having a predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

9. The multi-chip module system of claim 4, further comprising:

the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat; and

the third semiconductor device having a predetermined performance characteristic of at least substantially three times greater than that of the second predetermined performance characteristic of the second semiconductor device.

10. The multi-chip module system of claim 4, further comprising:

the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat; and

the third semiconductor device having a predetermined performance characteristic of at least substantially four times greater than that of the first and the second predetermined performance characteristic of the first semiconductor device and the second semiconductor device combined.

11. The multi-chip module system of claim 4, wherein the first semiconductor device comprises a memory device.

12. The multi-chip module system of claim 4, wherein the second semiconductor device comprises a memory device.

13. The multi-chip module system of claim 4, wherein the first semiconductor device comprises a microprocessor device.

14. The multi-chip module system of claim 4, wherein the second semiconductor device comprises a microprocessor device.

15. The multi-chip module system of claim 4, wherein the multi-chip module system comprises a single in-line memory module system.

16. The multi-chip module system of claim 4, further comprising:

a third semiconductor device; and

an adapter connected to the third semiconductor device, the adapter having a configuration for connecting the adapter to the at least one other vacant position on the substrate to connect the third semiconductor device to the substrate.

17. A multi-chip module system comprising:

a substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat, having a first vacant position having, in turn, a predetermined configuration for locating a third semiconductor device thereat, and having a second vacant position having, in turn, a predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system;

the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

the second semiconductor device located in the second position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic; wherein said first and second semiconductor devices have been burned in at said first and second positions, respectively, on said substrate.

18. The multi-chip system module of claim 17, wherein:

at least a portion of said substrate is substantially sheet-like, and wherein the first vacant position is located on the side of the substrate which is opposite the side upon which the second vacant position is located.

19. A multi-chip module system comprising:

a substrate having at least a first predetermined configuration position for locating a first semiconductor device thereat and having at least one other vacant predetermined configuration position for locating a second semiconductor device thereat on the multi-chip module system; and

the first semiconductor device located in the at least the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; wherein said first semiconductor device has been burned in at said first predetermined configuration position on said substrate.

20. The multi-chip module system of claim 19, further comprising:

the at least one other vacant predetermined configuration position for locating the second semiconductor device thereat which is substantially the same as the predetermined configuration of the first position.

21. The multi-chip module system of claim 19, further comprising:

the at least one other vacant predetermined configuration position having a predetermined configuration for locating the second semiconductor device thereat; and

the second semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

22. The multi-chip module system of claim 19, further comprising:

the at least one other vacant predetermined configuration position having a predetermined configuration for locating the second semiconductor device thereat; and

the second semiconductor device having a predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

23. A multi-chip module system comprising:

a substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor device thereat, and having at least one other vacant predetermined configuration position for locating a third semiconductor device thereat on the multi-chip module system;

the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

the second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic; wherein said first and second semiconductor devices have been burned in at said first and second predetermined configuration positions, respectively, on said substrate.

24. The multi-chip module system of claim 23, further comprising:

the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat which is substantially the same as the predetermined configuration of the first position.

25. The multi-chip module system of claim 23, further comprising:

the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat; and

the third semiconductor device having a third predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

26. The multi-chip module system of claim 23, further comprising:

the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat; and

the third semiconductor device having a third predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

27. The multi-chip module system of claim 23, further comprising:

the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat; and

the third semiconductor device having a third predetermined performance characteristic of at least substantially three times greater than that of the second predetermined performance characteristic of the second semiconductor device.

28. The multi-chip module system of claim 23, further comprising:

the at least one other vacant predetermined configuration position for locating a third semiconductor device thereat; and

the third semiconductor device having a third predetermined performance characteristic of at least substantially four times greater than that of the first and second predetermined performance characteristic of the first semiconductor device and the second semiconductor device combined.

29. The multi-chip module system of claim 23, wherein the first semiconductor device comprises a memory device.

30. The multi-chip module system of claim 23, wherein the second semiconductor device comprises a memory device.

31. The multi-chip module system of claim 23, wherein the first semiconductor device comprises a microprocessor device.

32. The multi-chip module system of claim 23, wherein the second semiconductor device comprises a microprocessor device.

33. The multi-chip module system of claim 23, wherein the multi-chip module system comprises a single in-line memory module system.

34. The multi-chip module system of claim 23, further comprising:

an adapter connected to the third semiconductor device, the adapter for connecting the adapter to the at least one other vacant predetermined configuration position on the substrate to connect the third semiconductor device to the substrate.

35. A multi-chip module system comprising:

a substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor device thereat, having a first vacant predetermined configuration position for locating a third semiconductor device thereat, and having a second vacant predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system;

the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

the second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic; wherein said first and second semiconductor devices have been burned in at said first and second predetermined configuration positions, respectively, on said substrate.

36. The multi-chip system module of claim 35, wherein:

at least a portion of said substrate is substantially sheet-like, and wherein the first vacant predetermined configuration position is located on the side of the substrate which is opposite the side upon which the second vacant predetermined configuration position is located.

REMARKS

Claims 1 through 36 are currently pending in the application.

This amendment is in response to the Office Action of August 12, 2002.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

Claims 2, 6, 18, 20, 24, and 36 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants have amended the claimed invention as suggested by the Examiner to particularly point out and distinctly claim the subject matter of the invention to comply with the provisions of 35 U.S.C. § 112. Therefore, presently amended claims 2, 6, 18, 20, 24, and 36 are allowable under the provisions of 35 U.S.C. § 112.

The Examiner asserts that claims 2, 6, 18, 20 and 24 do not conform to U.S.C. 112 in that "the scope of the limitation 'which is substantially the same as the first semiconductor device,' cannot be determined because the property that is the same is not recited or otherwise identified." However, the limitation is a valid structural constraint. The subject matter of Applicant's invention is intended to cover structures which contain semiconductor device positions which are configured alike and can receive semiconductor devices requiring such a configuration, regardless of the actual identity of the semiconductor device. Claims 2, 6, 20 and 24 have been amended to clearly reflect this valid structural limitation. Claim 18 does not contain the language to which the Examiner has objected, and Applicant presumes its inclusion is an oversight. The Examiner asserts that claims 18 and 36 do not conform to U.S.C. 112 in that there is "insufficient antecedent basis for the language 'the other side.'" The claims have been amended to correct the ambiguity. Applicant respectfully submits that claims 2, 6, 18, 20, 24 and 36 are in condition for allowance.

Claims 1 through 15, 17 through 33, 35, and 36 were rejected under 35 U.S.C. § 102(b) as being anticipated by Corbett (United States Patent 4,992,849).

Applicants submit that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

However, Applicants' claims have been amended to reflect the fact that the semiconductor devices in Applicants apparatus can be "burned in" after their assembly into modules. Specification page 5, paragraph 0017; Specification page 6, paragraph 0026. Applicant's apparatus simplifies the assembly of semiconductor devices into larger modules in that the die are not pre-burned in. With Applicant's invention a replacement semiconductor device can be attached to a vacant connection if an original semiconductor device fails during the burn in step. In contrast, the Corbett reference requires that the semiconductor devices be burned in before they are assembled into modules, even providing a separate apparatus for burn in, from which the semiconductor devices must be removed prior to their assembly into modules. Col. 3, Lines 3-30. Therefore, the Corbett reference does not describe the identical claimed invention of presently amended independent claim 1 in as complete detail as in the claim to anticipate the presently claimed invention under 35 U.S.C. § 102. Thus Applicant respectfully submits that claims1, 5, 17, 19, 23 and 35, as amended, are allowable. Claims 2 through 4 and 6 through 15 are allowable as depending directly from claim1, or indirectly, from claim 4. Claim 18 is allowable as depending from claim 17. Claims 20-22 are allowable as dependent from claim 19. Claims 24 through 33 are allowable as dependent from claim 23. Claim 36 is allowable as depending from claim 35.

Applicants further submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or

suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Claims 16 and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Corbett (UNITED States Patent 4,992,849) as applied to claims 1 through 15, 17 through 33, 35, and 36 above, and further in combination with Derouiche (United States Patent 5,623,395).

Applicant respectfully submits that claims 16 and 34 are allowable as depending from allowable claims. Furthermore, Applicants submit that claims 1 through 36 are clearly allowable over the cited prior art as the cited prior art cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of amended independent claims 1, 5, 17, 19, 23l, and 35. Applicants submit that the cited prior art fails to establish a *prima facie* case of obviousness under 35 U.S.C § 103 regarding the presently claimed invention of amended independent claim 1 because the combination of the cited prior art does not teach or suggest all the claim limitations of the presently claimed invention. As presently amended, independent claims 1, 5, 17, 19, 23, and 35 each clearly call for the claim limitation directed to " . . . said first semiconductor device being burned in at said location on said substrate." The combination of the cited prior art clearly fails to teach or suggest such claim limitations to establish a *prima facie* case of obviousness under 35 US.C. § 103 regarding the presently claimed invention of amended independent claims 1, 5, 17, 19, 23, and 35. Therefore, such amended independent claims and all the dependent claims therefrom are allowable.

In summary, for the reasons set forth herein, Applicants request the allowance of claims 1 through 36 and the case passed for issue.

Respectfully submitted,

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Enclosure: Version with Markings to Show Changes Made

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